Skylake Front-end Architecture

Haswell Front-end

- Branch Prediction Unit
- L1 Instruction Cache
- 16Bytes
- uOP Cache Hit Logic
- Instruction Fetch and PreDecode
- Instruction Queue
- uOP Cache
- MicroCode ROM
- 4-way Decode (Micro-Fusion/Macro-Fusion)
  - Complex Decoder
  - Simple Decoder
  - Simple Decoder
  - Simple Decoder
- 4 uOPs
- 4 uOPs
- Allocation Queue
- 4 uOPs
- Rename/Allocate/Retirement

Skylake Front-end

- Branch Prediction Unit
- L1 Instruction Cache
- 16Bytes?
- uOP Cache Hit Logic
- Instruction Fetch and PreDecode
- Instruction Queue
- uOP Cache
- MicroCode ROM
- 5-way Decode (Micro-Fusion/Macro-Fusion)
  - Complex Decoder
  - Simple Decoder
  - Simple Decoder
  - Simple Decoder
  - Simple Decoder
- 6 uOPs
- 5 uOPs
- Allocation Queue
- 6 uOPs
- Rename/Allocate/Retirement