				Channel 3 HBM DRAM	M Core Die 3			Channel 7	2Channel/D
TSV+ TSV+ TSV+				TSV S	tacking				•
			Channel 2	HBM DRAI	M Core Die 2		Channel 6		2Channel/D
TSV+ NicroBump				TSV S	tacking				
		Channel 1		HBM DRAM	/ Core Die 1	Channel 5			2Channel/D
TSV+ † MicroBump				TSV S	tacking				
	Channel 0			HBM DRAI	Channel 4 I Core Die 0				2Channel/D
TSV+ MicroBump	Channel 0	Channel 1	Channel 2		Stacking Channel 4 4 bits	Channel 5	Channel 6	Channel 7	
	← —128 bits——	← —128 bits——	← —128 bits——	128 bits	+ bits — 128 bits — →	←—128 bits——	← —128 bits——	← —128 bits——	
	Memory Channel 0	Memory Channel 1	Memory Channel 2	Memory Channel 3 Base L	Memory Channel 4 ogic Die	Memory Channel 5	Memory Channel 6	Memory Channel 7	Optional Logic Die
Interposer #	Channel 0	Channel 1	Channel 2	TSV Ir Channel 3	terposer Channel 4 4 bits	Channel 5	Channel 6	Channel 7	
	← —128 bits——	← —128 bits——	← —128 bits——	128 bits	+ bits ————————————————————————————————————	← —128 bits——	← —128 bits——	← —128 bits——	
	Memory Channel 0	Memory Channel 1	Memory Channel 2	Memory Channel 3	Memory Channel 4	Memory Channel 5	Memory Channel 6	Memory Channel 7	
				Controller (G	PU/CPU/SoC)				