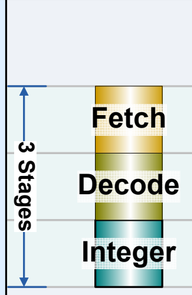
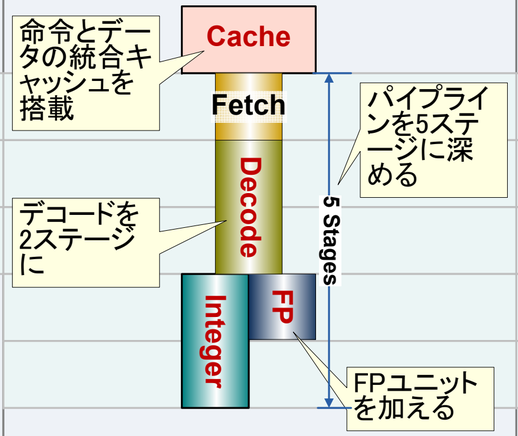
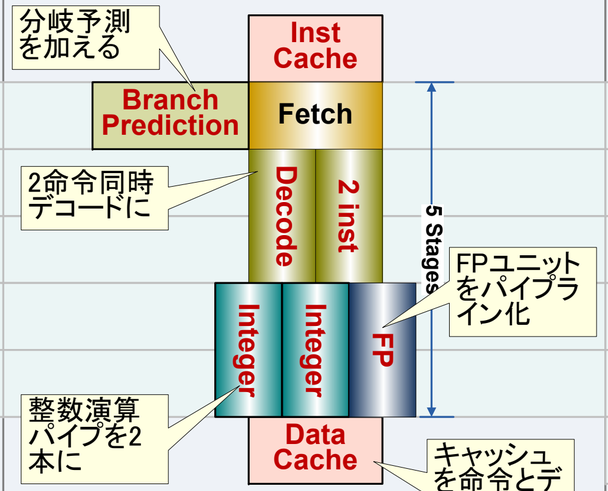
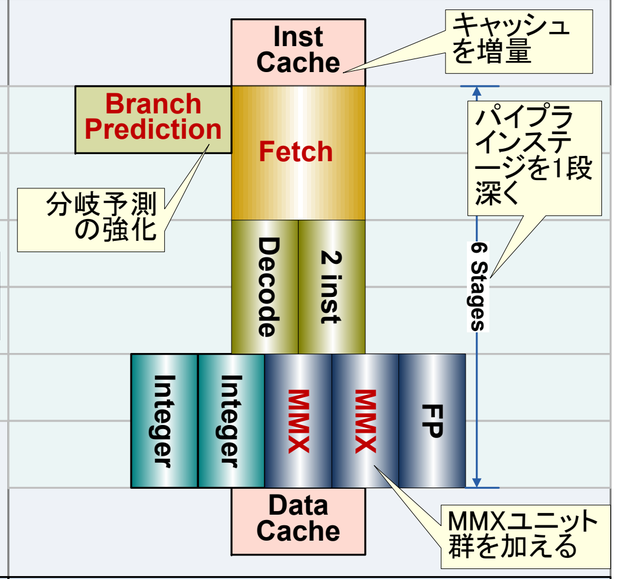
386 to P55C Architecture Evolution

	386DX	486DX	Pentium(P5)	Pentium MMX(P55C)
				
Pipeline Stages	3	5	5	6
Instruction Cache	N/A	8KB	8KB	16KB
Data Cache	N/A		8KB	16KB
Instruction Decode	1	1	2	2
Frequency	～33MHz	～100MHz(486DX4)	～200MHz(P54CS)	～300MHz(Tillamook)
Floating Point Unit	N/A(387)	Non-Pipelined FP	Pipelined FP	Pipelined FP
Branch Prediction	N/A	N/A	Branch Target Buffer	Branch Target Buffer /Return Stack Buffer
Data Bus	32-bit	32-bit	64-bit	64-bit
Introduction Year	1985	1989	1993	1997
Transistors	275K	1.2M	3.1M	4.5M
Process Technology	1.5->1μm	1μm->800->600nm	800->600->350nm	350->280->250nm