Bonnell Pipeline

	Memory+Integer	
1	Instruction Fetch	IF1
2		IF2
3		IF3
4	Instruction Decode	ID1
5		ID2
6		ID3
7	Instruction Dispatch	SC
8		IS
9	Source Operand Read	IRF
10	Address Generation	AG
11	Data Cache Access	DC1
12		DC2
13	Execute	EX1
14	Exceptions and Multithread handling	FT1
15		FT2
16	Commit	IWB/DC1

13-cycle Branch Mispredict Latency

Silvermont Pipeline

	Integer		Memory Access	
1	Instruction Fetch	IF1		
2		IF2		
3		IF3		
4	Instruction Decode	ID1		
5		ID2		
6		ID3		
7	Allocate Rename	AR1		
8		AR2		
9	Schedule	RSV	RSV	Schedule
10	Execute	EX	AG	Address Generation
11	Retire	RB1	DC1	Data Cache Access
12		RB2	DC2	
13	Commit	RB3		
14		RB4		

10-cycle Branch Mispredict Latency