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ARM Cortex-A57 Block Diagram

Non-Processor / Level 2 Shared L2 Cache
512KB/1MB/2MB (16-way set-associative ECC)

L2 Arbitration
Fill/Evict Buffer

AXI Coherency Extensions (ACE)

Snoop Master

Snoop Slave

TAG RAM

Prefetch Engine

Accelerator Coherency Port (ACP)

Cortex-A57 Processor Core
L1 Instruction Cache
48KB (3-way set-associative / 64-Byte cache line / Parity)

32-entry Loop Buffer
Dispatch States
Issue (8-entry Queue per Issue port)

Instruction Fetch
3-way Instruction Decode
Register Rename
Virtual to Physical Register Pool

Load/Store Simple Cluster 1
Complex Cluster (NEON/FPU)

Multiply, MAC
Divide Cluster

Load/Store Simple Cluster 0
Complex Cluster (NEON/FPU)

Branch

Branch Prediction
Global History Buffer
Branch Target Buffer (BTB)(2k-4k)
Return Stack MicroBTB (64-entry)
Indirect Predictor w/path history

L2 TLB (512-entry)
Processor Arbitration (1ST Level)
Load TLB (32-entry)
Store TLB (32-entry)

Bi-mode Predictor

48-bit Virtual Address
44-bit Physical Address

All NEON & FPU ops QUad-FMAC

ARM multiply & Integer divide, MAC
Integer ALU & Shifter (includes v6-SIMD)

L1 Data Cache
32KB ECC (2-way set-associative / 64-byte cache line)

Load-Store Unit
Store Buffer

WriteBack 128 micro-ops in-flight

Retirement Buffer 128 bits

12 Stage In-Order Pipeline
3-12 Stage Out-of-Order Pipeline
Up to 8 micro-ops Issue

Commit