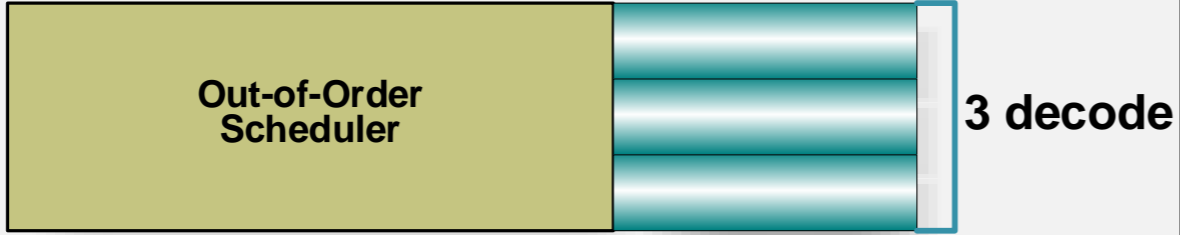
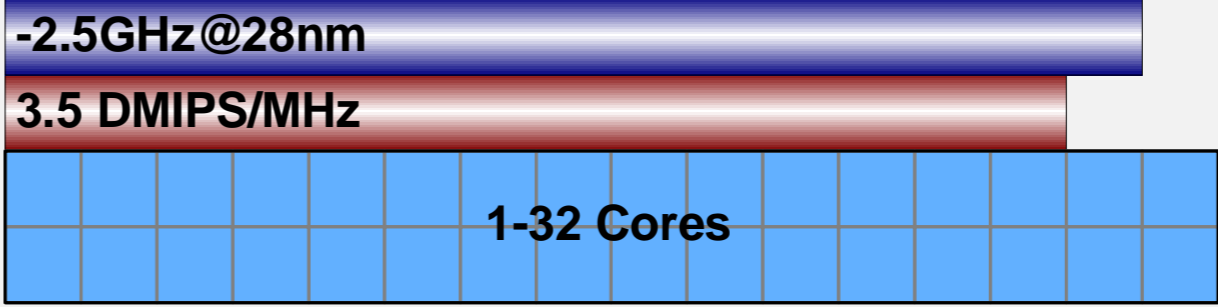
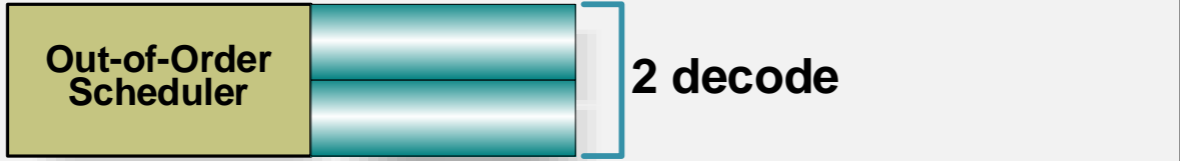
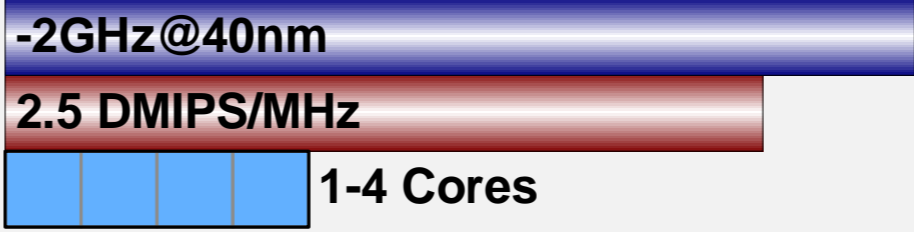
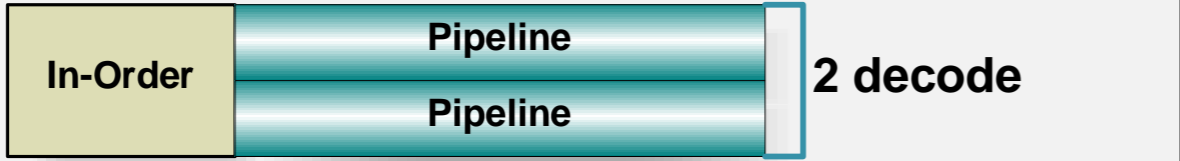
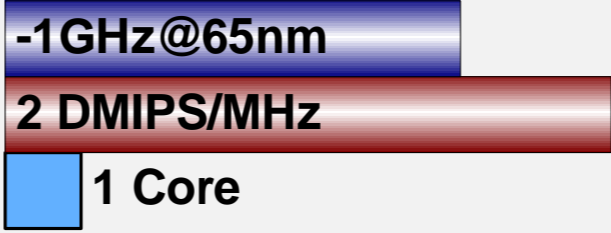

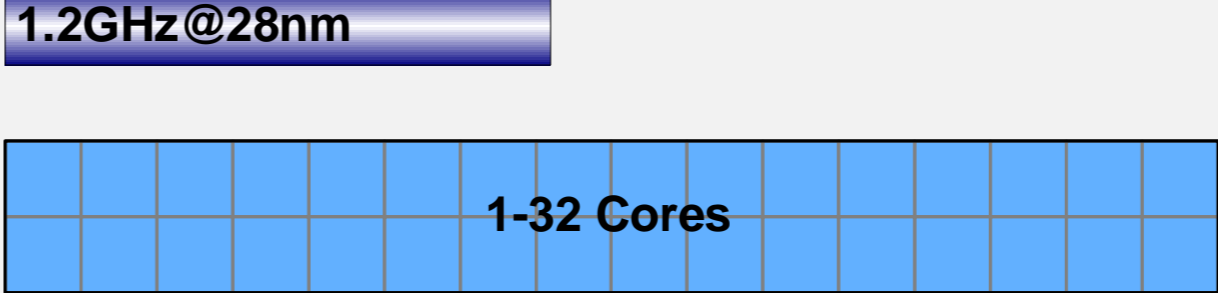
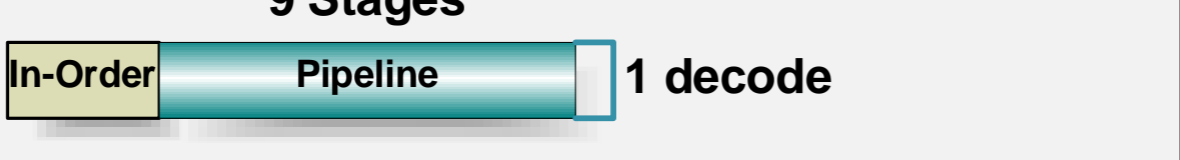
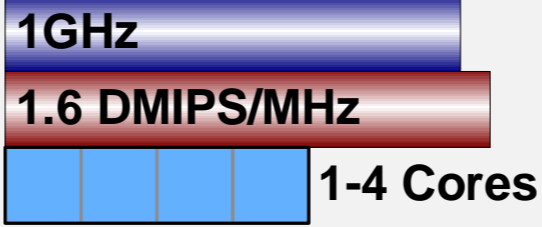


ARM Cortex-A Family Architecture

<p>Cortex-A15</p>	<p>15+ Stages</p>  <p>Out-of-Order Scheduler 3 decode</p>	<p>-2.5GHz@28nm</p> <p>3.5 DMIPS/MHz</p> <p>1-32 Cores</p> 
<p>Cortex-A9</p>	<p>9-12 Stages</p>  <p>Out-of-Order Scheduler 2 decode</p>	<p>-2GHz@40nm</p> <p>2.5 DMIPS/MHz</p> <p>1-4 Cores</p> 
<p>Cortex-A8</p>	<p>13 Stages</p>  <p>In-Order Pipeline Pipeline 2 decode</p>	<p>-1GHz@65nm</p> <p>2 DMIPS/MHz</p> <p>1 Core</p> 
<p>Cortex-A7</p>	<p>8 Stages</p>  <p>In-Order Limited 2 decode</p>	<p>1.2GHz@28nm</p> <p>1-32 Cores</p> 
<p>Cortex-A5</p>	<p>9 Stages</p>  <p>In-Order Pipeline 1 decode</p>	<p>1GHz</p> <p>1.6 DMIPS/MHz</p> <p>1-4 Cores</p> 

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