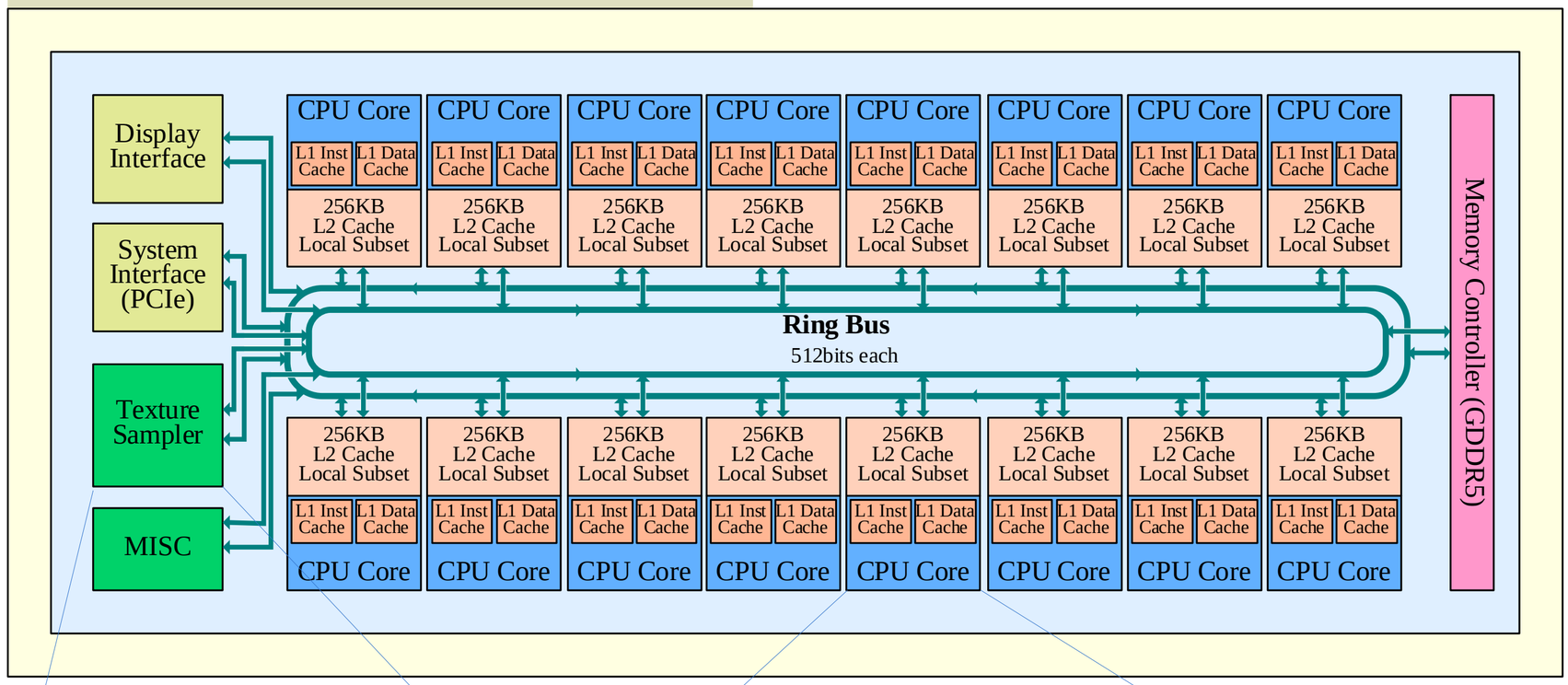
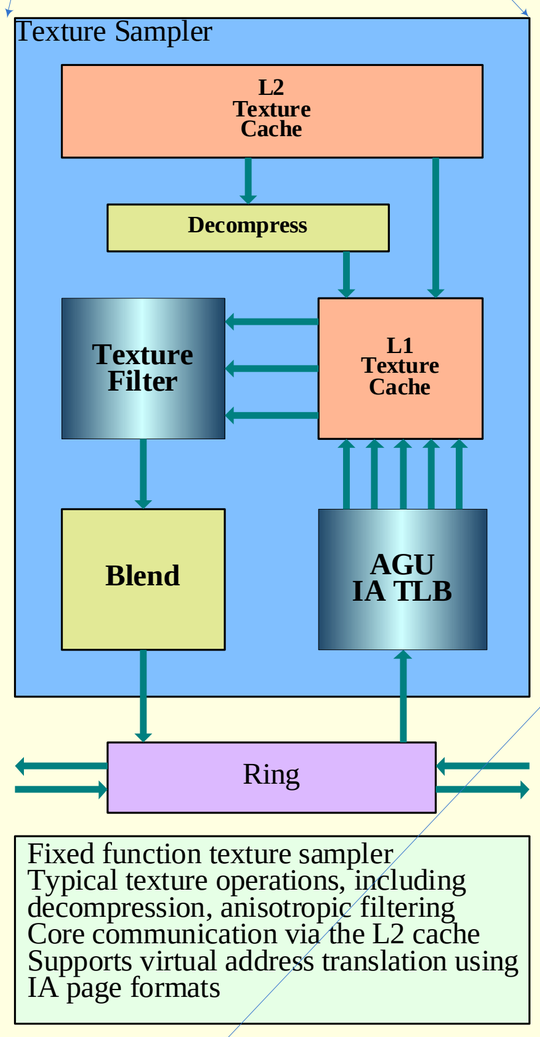
Larrabee 1 Architecture

Larrabee

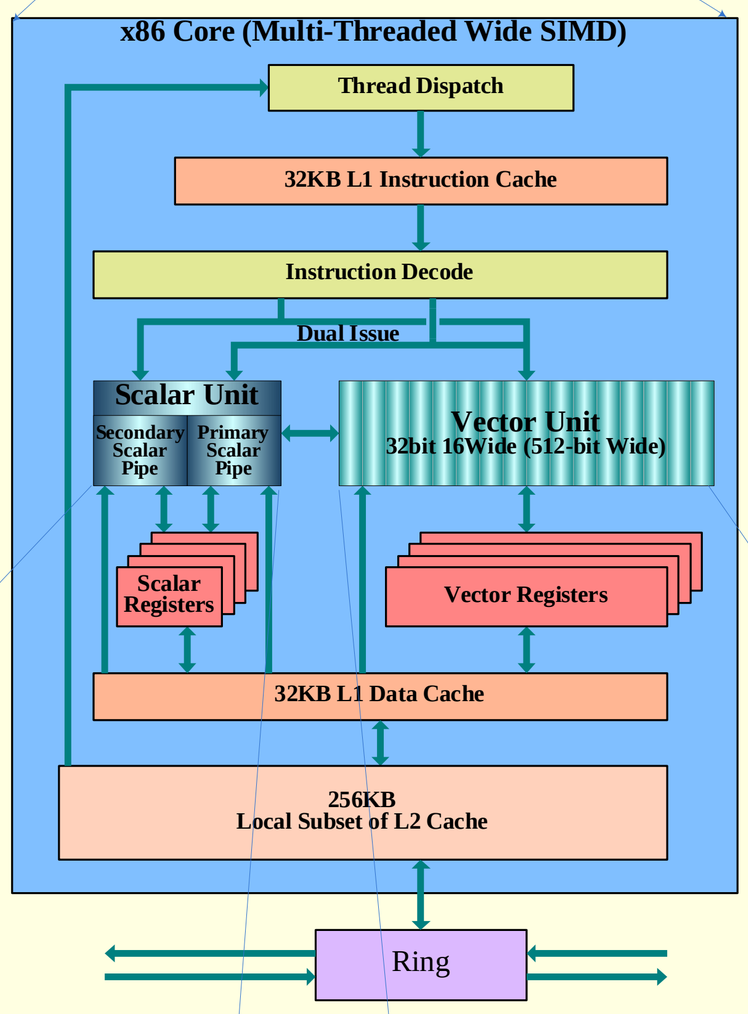


Texture Sampler



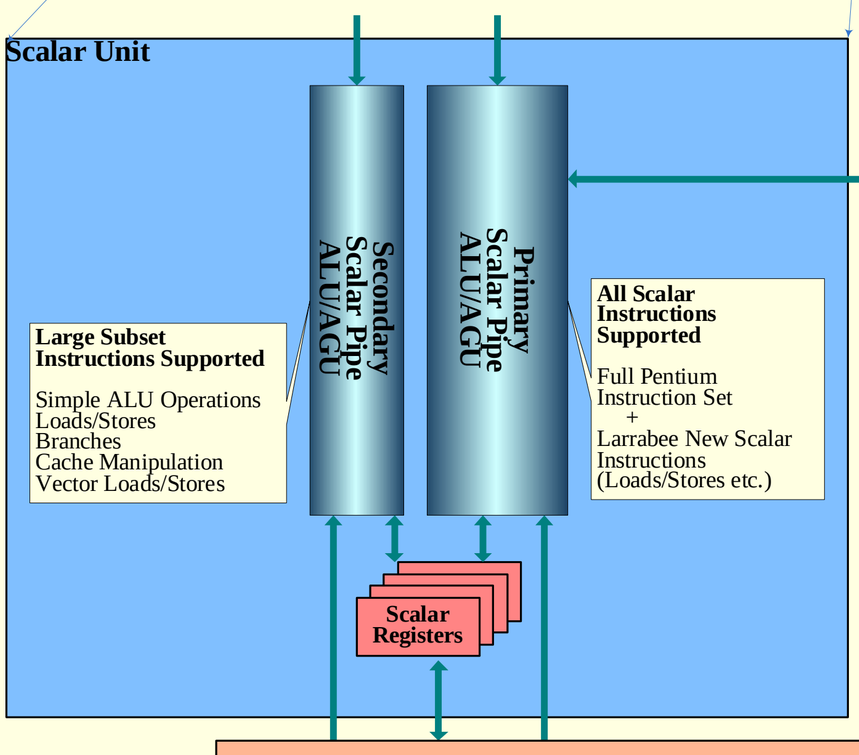
Fixed function texture sampler
Typical texture operations, including decompression, anisotropic filtering
Core communication via the L2 cache
Supports virtual address translation using IA page formats

x86 Core (Multi-Threaded Wide SIMD)



In-order x86 CPU core
4-way multithreading
64-bit mode
Separated scalar and vector units
Separated scalar and vector registers
Vector unit: 16 32-bit ops/clock
Short execution pipelines
Fast access from L1 cache
Direct connection to each core's subset of the L2 cache
Prefetch instructions load L1 and L2 caches

Scalar Unit



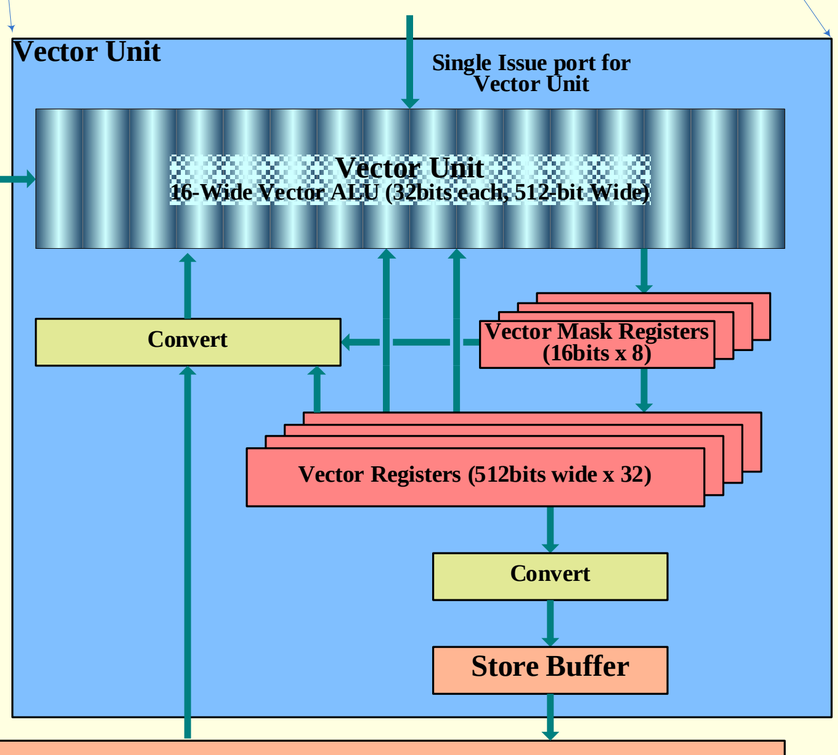
Large Subset Instructions Supported

Simple ALU Operations
Loads/Stores
Branches
Cache Manipulation
Vector Loads/Stores

All Scalar Instructions Supported

Full Pentium Instruction Set
+
Larrabee New Scalar Instructions (Loads/Stores etc.)

Vector Unit



32KB L1 Data Cache (64Bytes=512bits Cache Line)

Vector complete instruction set
Scatter/gather for vector load/store
Mask registers select lanes to write (for data-parallel flow control)
A separate execution kernel to each VPU lane

Vector instructions support
Fast read from L1 cache
Numeric type conversion and data replication (read path from memory)
Rearrange the lanes on register read
Fused multiply add (three arguments)
Int32, Float32 and Float64 data