Cell Broadband Engine (BE) in PS3 high level diagram

Cell Broadband Engine (BE)

PPU (Power Processor Unit)
- L1 cache
- L2 cache
- 256-bit/cycle
- PXU (Power core)

Memory Interface Controller (MIC)

Bus Interface Controller (BIC)
128-bit/cycle

Element Interconnect Bus (EIB) Rings (768-bit/cycle)

SPU (Synergistic Processor Unit)
- Local Store (LS)
- SXU (SIMD)

XIO (Dual XDR Interface)

XDR DRAM 512Mb

FlexIO

I/O Bridge

RSX (Reality Synthesizer)

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