AMD 32nm K10 CPU Core

Instruction Fetch Decode Branch

Integer Execution Unit

Load Store Unit

Power-Gate Ring

L1 Instruction Cache 64KB

Bus Interface (L2 Controller)

L1 Data Cache 64KB
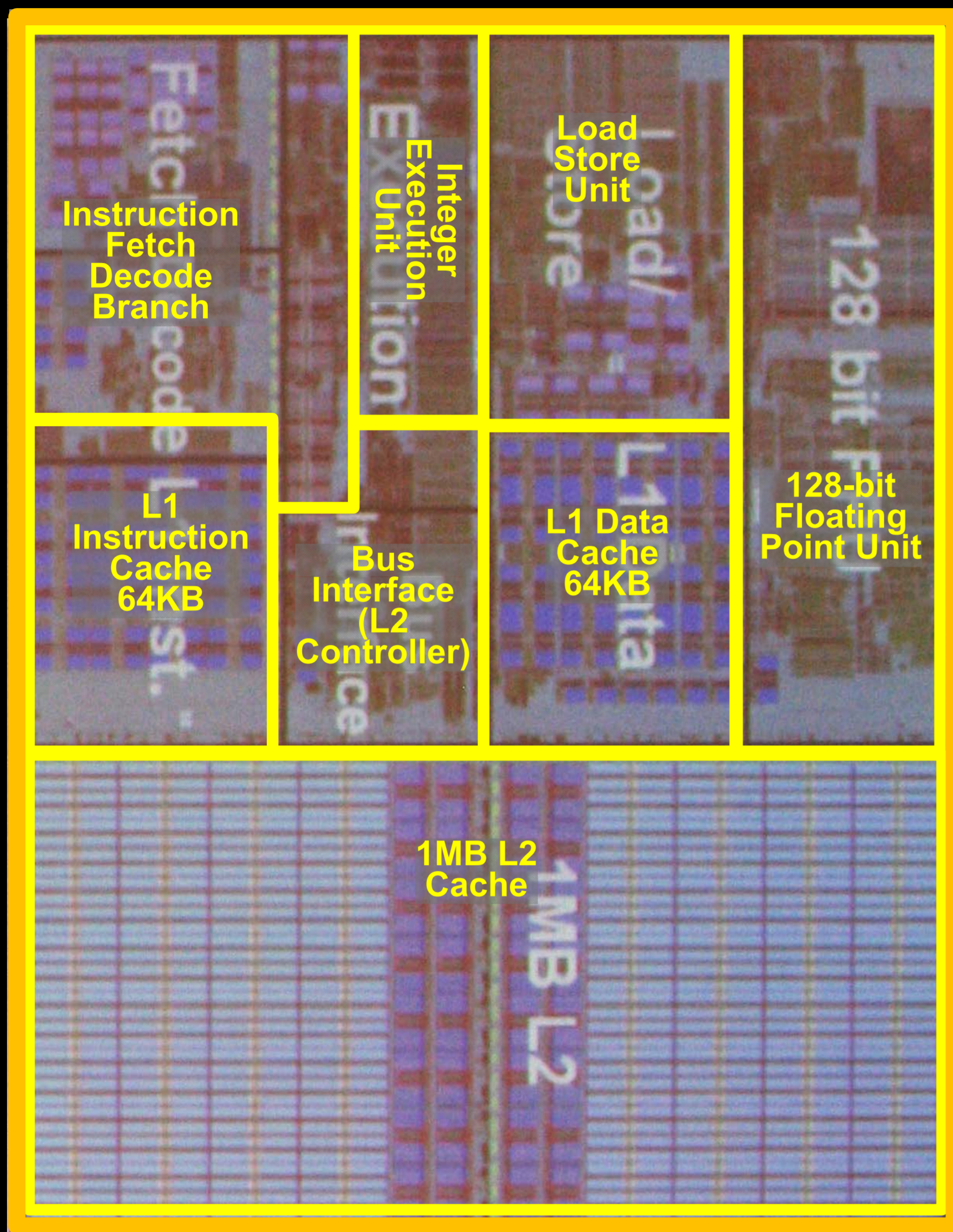
128-bit Floating Point Unit

1MB L2 Cache

Process
 32nm high-k metal-gate (HKMG) SOI Process
Core
 9.69mm2
 35 M Transistors
Core + 1MB L2 + Power-Gate Ring
 17.7mm2
 110 M Transistors
Voltage
 0.8 - 1.3V
Power
 2.5 − 25W
Frequency
 >3GHz

Architectural Improvements

Bigger instruction window For more integer/FP execution throughput
 (72-entry to 84-entry)
Hardware integer divide
Lower latency FP instructions
Enhanced data prefetching
Faster memory fills and cache state transitions
I/O-based C-states including full processor state save
Enhanced TLB residency for virtualization