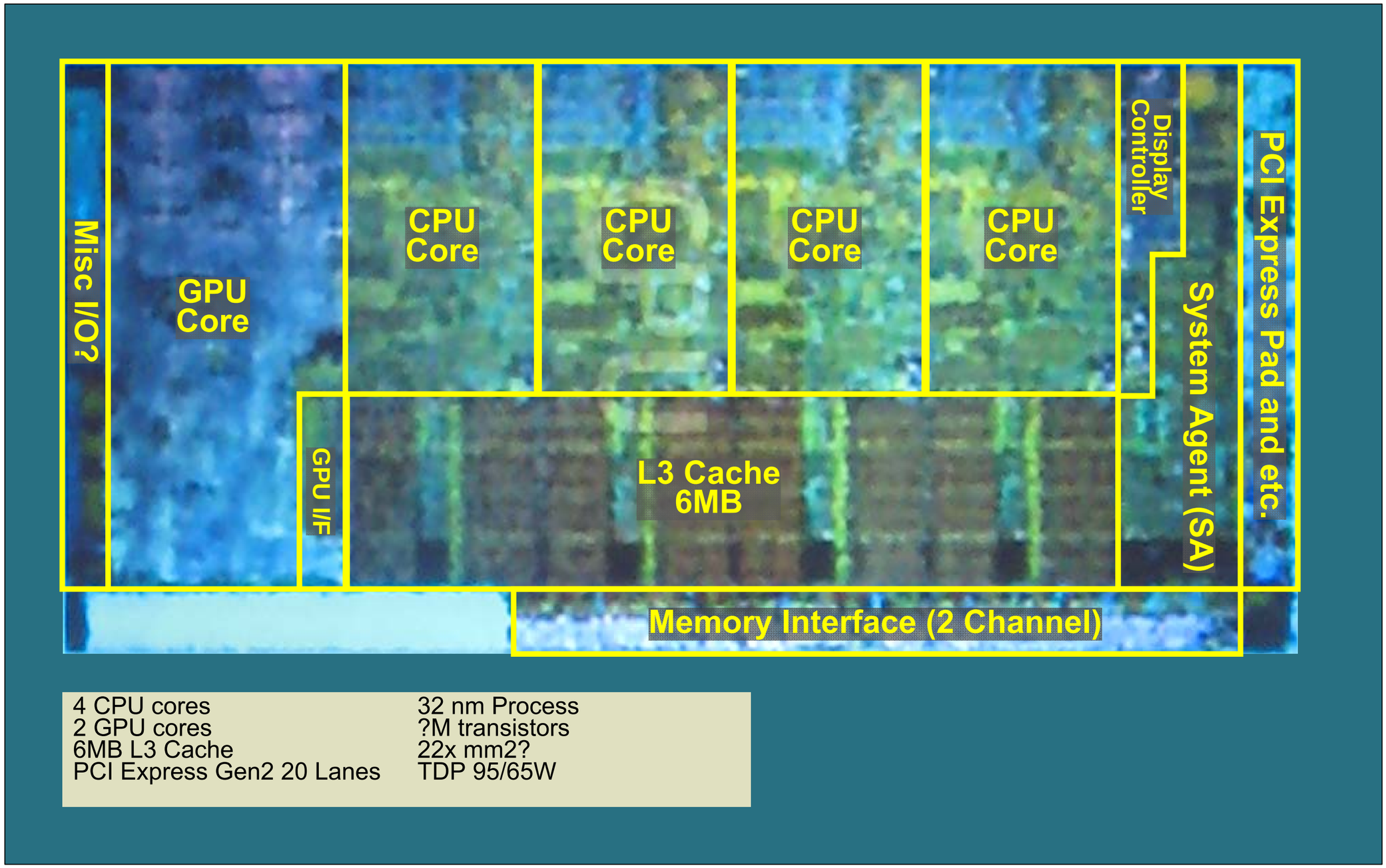
Sandy Bridge Die Layout (Estimated)



4 CPU cores	32 nm Process
2 GPU cores	?M transistors
6MB L3 Cache	22x mm2?
PCI Express Gen2 20 Lanes	TDP 95/65W