	ISSCC 2017, B. Moons, ENVISION [5]	VLSI 2018, Z. Yuan, STICKER [6]	ISSCC 2018, J.Lee, UNPU [7s]	Proposed*		
				1 Chip	4 Chip (2 × 2)	36 Chip (6 × 6)
Technology	28nm	65nm	65nm	16nm		
Cumulative Core Area	1.87 mm^2	7.8 mm^2	13 mm^2	3.1 mm^2	12.4 mm^2	111.6 mm^2
Cumulative Die Area	unknown	12 mm^2	16 mm^2	6 mm^2	24 mm^2	216 mm^2
Precision	4b,8b,16b	8b	1-16b	8b		
On-Chip SRAM (MB)	0.14	0.17	0.25	0.625	2.5	22.5
Supply Voltage (V)	1	0.67-1.1	0.63-1.1	0.41-1.2	0.52-1.2	0.52-1.1
Frequency (MHz)	200	200	5-200	161-2001	515-1998	484-1797
Core Power (mW)	165	21-248	3.2-297	30-4160	630-16,420	5,310-106,090
GRS Power† (mW)	n/a	n/a	n/a	n/a	215-220	3,840-4,090
MACs per cycle	512 @8b	256	1,728@8b	1,024	4,096	36,864
Performance (TOPS)	~0.15@8b	0.1	0.69@8b	0.32-4.01	3.93-15.7	32.5-127.8
Core Energy Efficiency (pJ/op)	~1.1@8b	0.96	~0.18@8b	0.105-1.04	0.160-1.05	0.164-8.30
Core Area Efficiency (TOPS/mm^2)	0.08	0.013	0.053	0.10-1.29	0.32-1.27	0.29-1.15

* Measured results reported for 40% density weights and input activations †11Gbps mode

Fig. 9: Comparison table.