

10nm Process Feature Size

凡例	Intel 10nm	TSMC 10FF	Samsung 10LPE	Samsung 10LPP
<p>Legend diagram showing a cross-section of a finFET. Labels include: Gate Pitch/CPP (width of gate), Metal (blue layer), Fin (orange layer), Gate (green layer), Minimum Metal Pitch (width of metal), and Fin Pitch (width of fin).</p>	<p>Intel 10nm finFET cross-section. Dimensions: Gate Pitch/CPP = 54nm, Minimum Metal Pitch = 36nm, Fin Pitch = 34nm.</p>	<p>TSMC 10FF finFET cross-section. Dimensions: Gate Pitch/CPP = 66nm, Minimum Metal Pitch = 44nm, Fin Pitch = 36nm.</p>	<p>Samsung 10LPE finFET cross-section. Dimensions: Gate Pitch/CPP = 64nm, Minimum Metal Pitch = 48nm, Fin Pitch = 42nm.</p>	<p>Samsung 10LPP finFET cross-section. Dimensions: Gate Pitch/CPP = 64nm, Minimum Metal Pitch = 44nm, Fin Pitch = 42nm.</p>