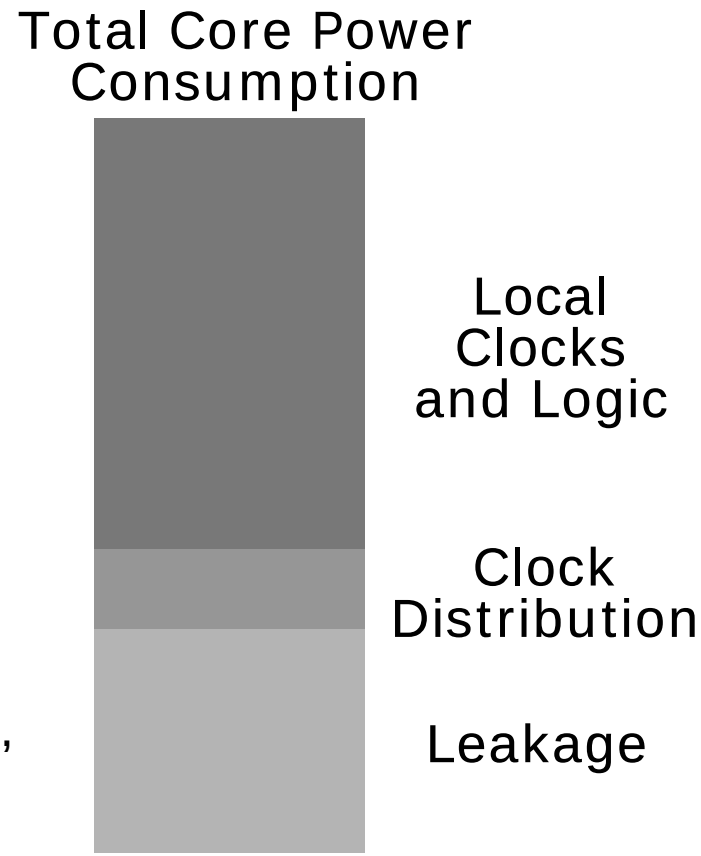
CPU Core Power Consumption

- Remaining power in logic, local clocks
  - Power efficient microarchitecture, good clock gating minimize waste
- High frequency designs require high performance global clock distribution
- High frequency processes are leaky
  - Reduced via high-K metal gate process, design technologies, manufacturing optimizations



Challenge – Minimize power when idle