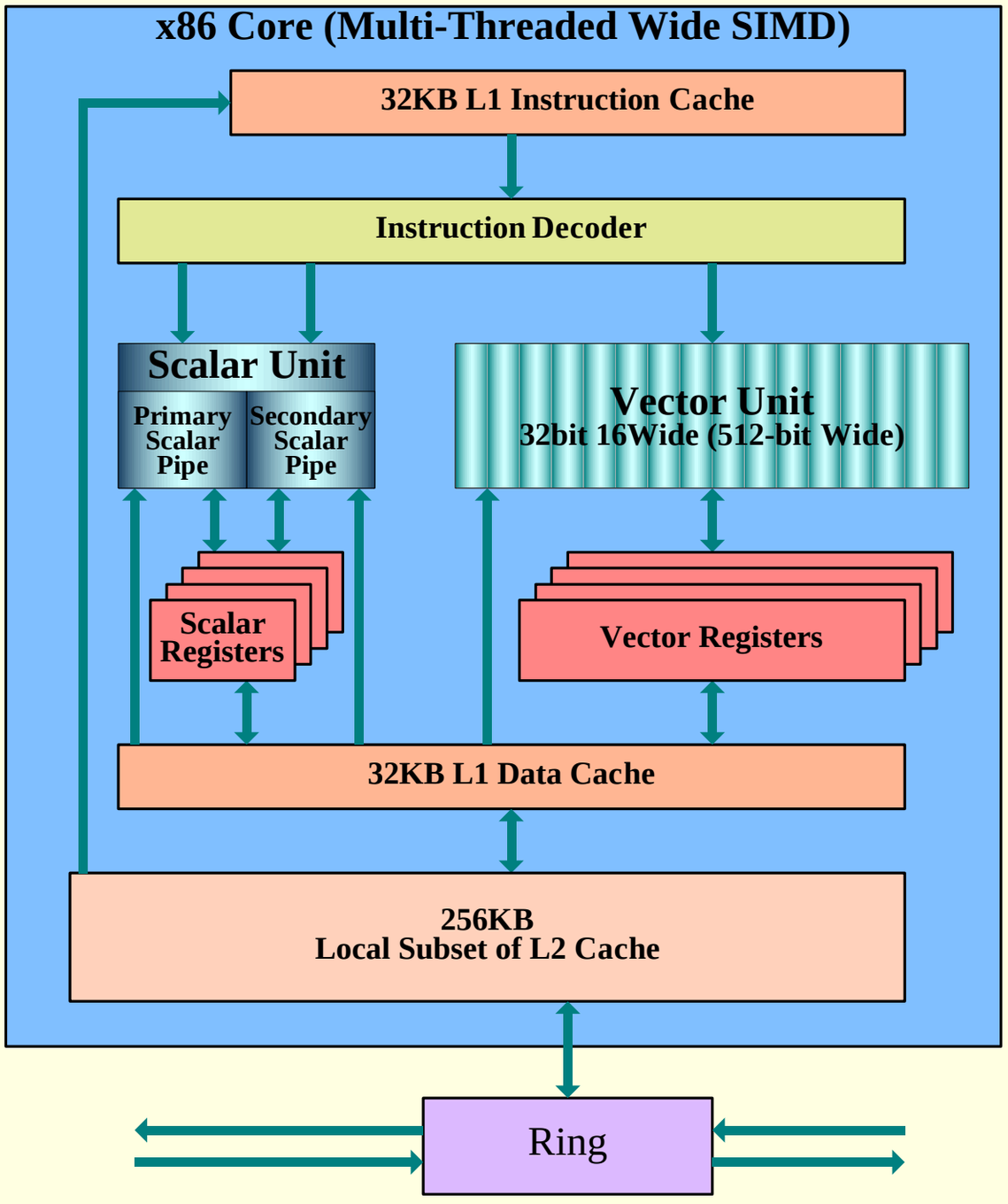
Larrabee x86 Core Block Diagram



In-order x86 CPU core
4-way multithreading
Separated scalar and vector units
Separated scalar and vector registers
Vector unit: 16 32-bit ops/clock
Short execution pipelines
Fast access from L1 cache
Direct connection to each core's subset of the L2 cache
Prefetch instructions load L1 and L2 caches