

Delivering more DRAM bandwidth

- Independent DRAM controllers
- Optimized DRAM paging
- Re-architect NB for higher BW
- Write bursting
- DRAM prefetcher
- **Core prefetchers**

- ▶ **DC Prefetcher fills directly to L1 Cache**
- ▶ **IC Prefetcher more flexible**
 - ▶ 2 outstanding requests to any address