2. Chip Multiprocessor (CMP) Generations

- *Generation-0*
  - *Hasty integration of a bunch of cores*
  - *Jam multiple single core devices into the same package*
- ***Generation-1***
  - Design from the ***system-level inward***
  - Balanced integration of cores and system functionality
  - Address ***HW scalability*** inhibitors
- ***Generation-2***
  - Understand and address ***interference*** issues *(destructive & constructive)*
  - ***Chip-level framework*** & infrastructure to support range of CMP variants
  - Improve ***SW visibility*** & ***optimization*** for parallel application development
- ***Generation-3***
  - Introspective self-management
  - Runtime adaptive flexibility
    - *Specialized resources and optimizations*
    - *Engage resources appropriate for each application*