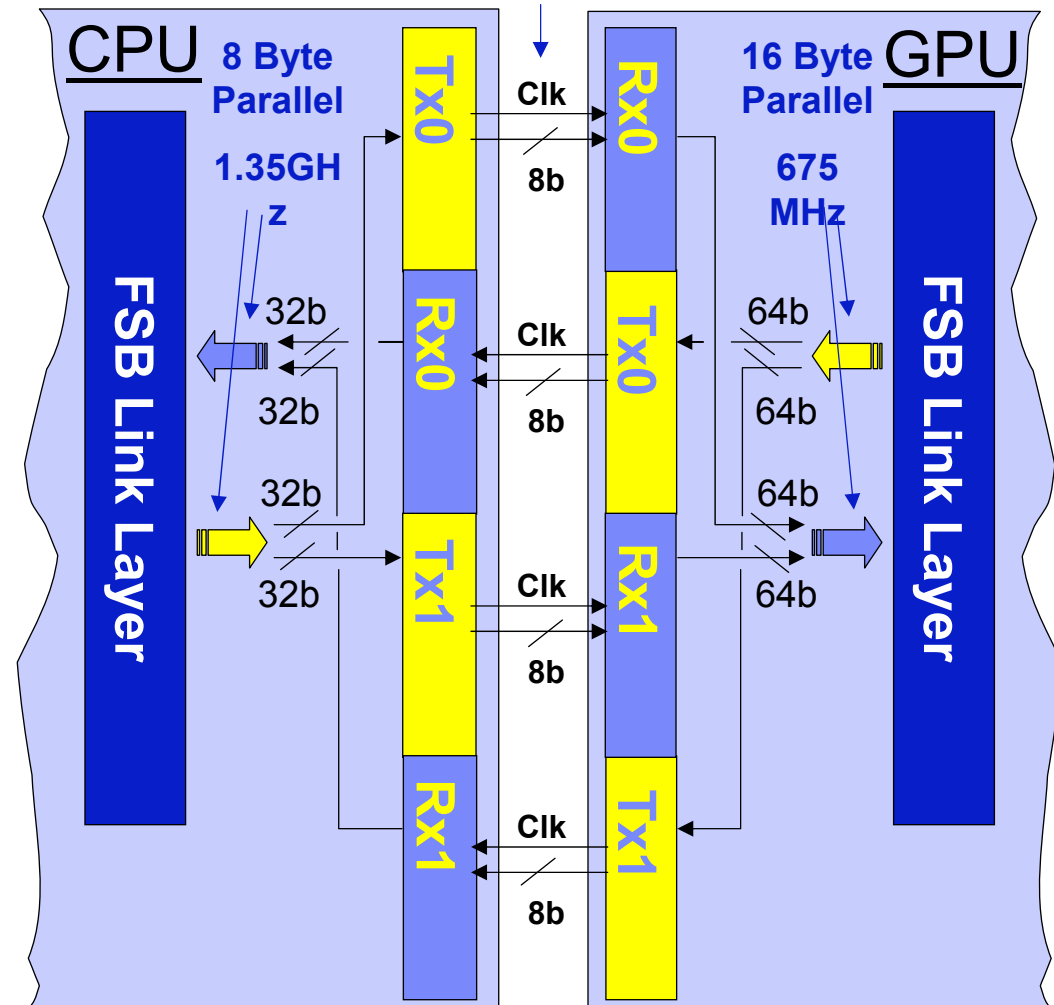


Front Side Bus – Physical Layer

- 4:1 & 8:1, 5.4 Gb/s SerDes
 - Source Synchronous
 - 2 byte, full duplex operation
 - IBM SOI CMOS 10KE (CPU)
 - TSMC 90GT (GPU)
- 1.1V CML Based Design
 - Dynamic termination to 50 ohms
 - Low Jitter, High Noise Tolerance
- Low cost packaging
 - Organic Substrate
 - 2/2/2 on CPU
 - 3/2/3 on GPU
 - 2s, 2p System Card
 - 6 inches of wire

5.4Gb/s data rate per bit lane (x32 lanes) + 1 CLK per byte Lane(4)



1st Pass Hardware Performance:

- Tx Eye Diagram
- Rx Packet Error Rate Bathtub

