Sustaining High Memory Bandwidth

- ## Optimized Main TLB for performance
  - Main TLB prefetcher for large workload streaming
  - 2 simultaneous Page Table Walks
  - Ability to hit in TLB during PTW

- ## L2 cache optimisations
  - Sustain parallel streams with no performance loss for better multi-core performance scaling
  - Decorrelated Cacheable and Non-Cacheable accesses
  - Enhanced arbitration for interleaving accesses
  - Improved and smart cache replacement policy

ARM