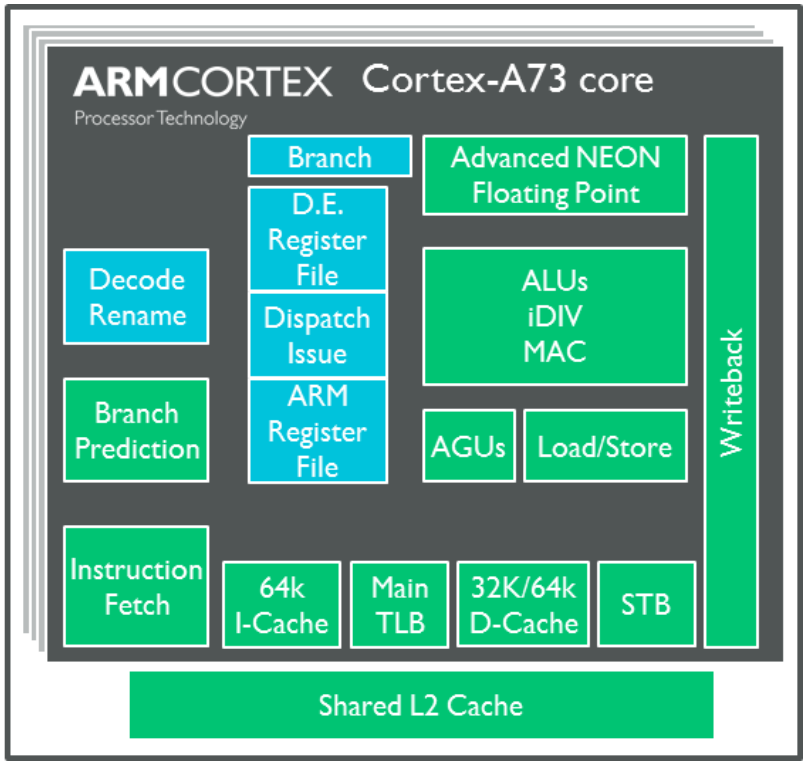
Efficient 2-wide Superscalar Engine

- Dual Decode for power efficiency and performance
  - Instruction-fusion capability
  - Reduced set of instructions split into Micro-OPs
- Out-of-order branch capability
- Optimized issuing and renaming resources
  - Resource sharing improved for AArch64 and AArch32 for area and power reduction
  - Low-level optimization for Data Engine for timing and performance improvement
  - Improved issue-queue load-balancing algorithm



EMBARGOED UNTIL 11pm EDT on Sunday, May 29

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