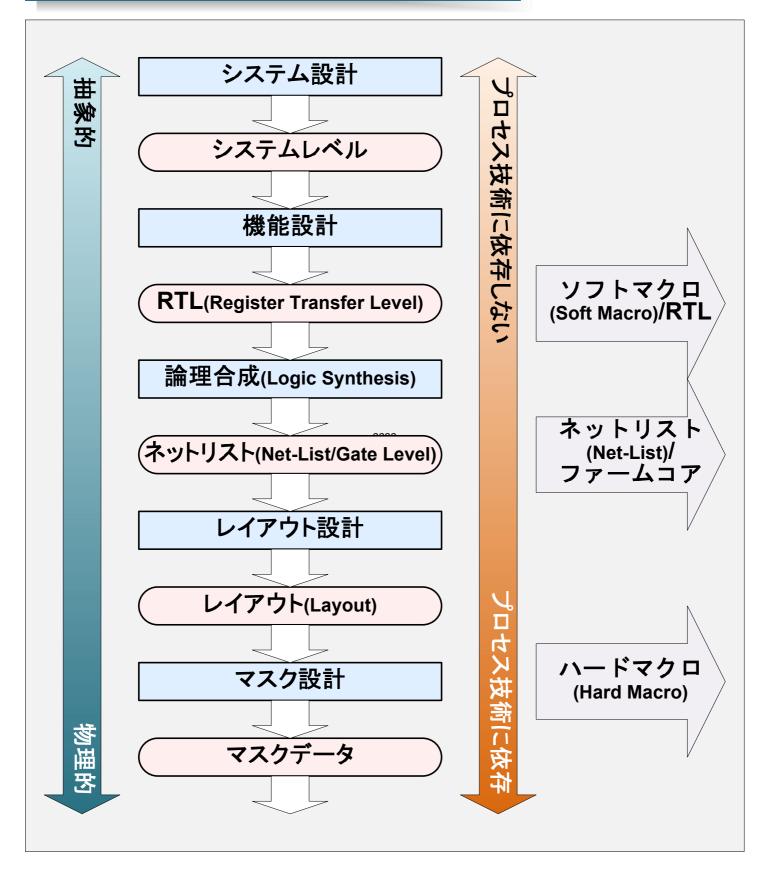
論理合成する場合のLSI設計のフロー



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