HBM Architecture

| | | | | Channel 3 HBM DRAN | Core Die 3 | | | Channel 7 | 2Channel/ |
|---------------------|------------------|------------------|----------------------|---------------------------------|------------------------------|------------------|------------------|------------------|--------------------|
| TSV+ T VicroBump | | | | TSV S | acking | | | | |
| | | | Channel 2 | HBM DRAN | Core Die 2 | | Channel 6 | | 2Channel |
| TSV+ TicroBump | | | | TSV St | tacking | | | | |
| | | Channel 1 | | HBM DRAN | Core Die 1 | Channel 5 | | | 2Channel |
| TSV+ ¶ | | | | TSV St | tacking | | | | |
| | Channel 0 | | | HBM DRAN | Channel 4 I Core Die 0 | | | | 2Channel |
| TSV+ licroBump | Channel 0 | Channel 1 | Channel 2 | | tacking Channel 4 | Channel 5 | Channel 6 | Channel 7 | |
| | 128 bits | 128 bits | 128 bits | 102¬ | 128 bits | 128 bits | 128 bits | 128 bits | |
| | Memory Channel 0 | Memory Channel 1 | Memory Channel 2 | Memory Channel 3 Base Lo | Memory Channel 4 | Memory Channel 5 | Memory Channel 6 | Memory Channel 7 | Optiona Logic D |
| Interposer # | Channel 0 | Channel 1 | Channel 2 | TSV In Channel 3 | terposer Channel 4 | Channel 5 | Channel 6 | Channel 7 | |
| | 128 bits | 128 bits | ← —128 bits—— | 102¬ | 128 bits | 128 bits | 128 bits | 128 bits | |
| | Memory Channel 0 | Memory Channel 1 | Memory Channel 2 | Memory Channel 3 Controller (G | Memory Channel 4 PU/CPU/SoC) | Memory Channel 5 | Memory Channel 6 | Memory Channel 7 | |