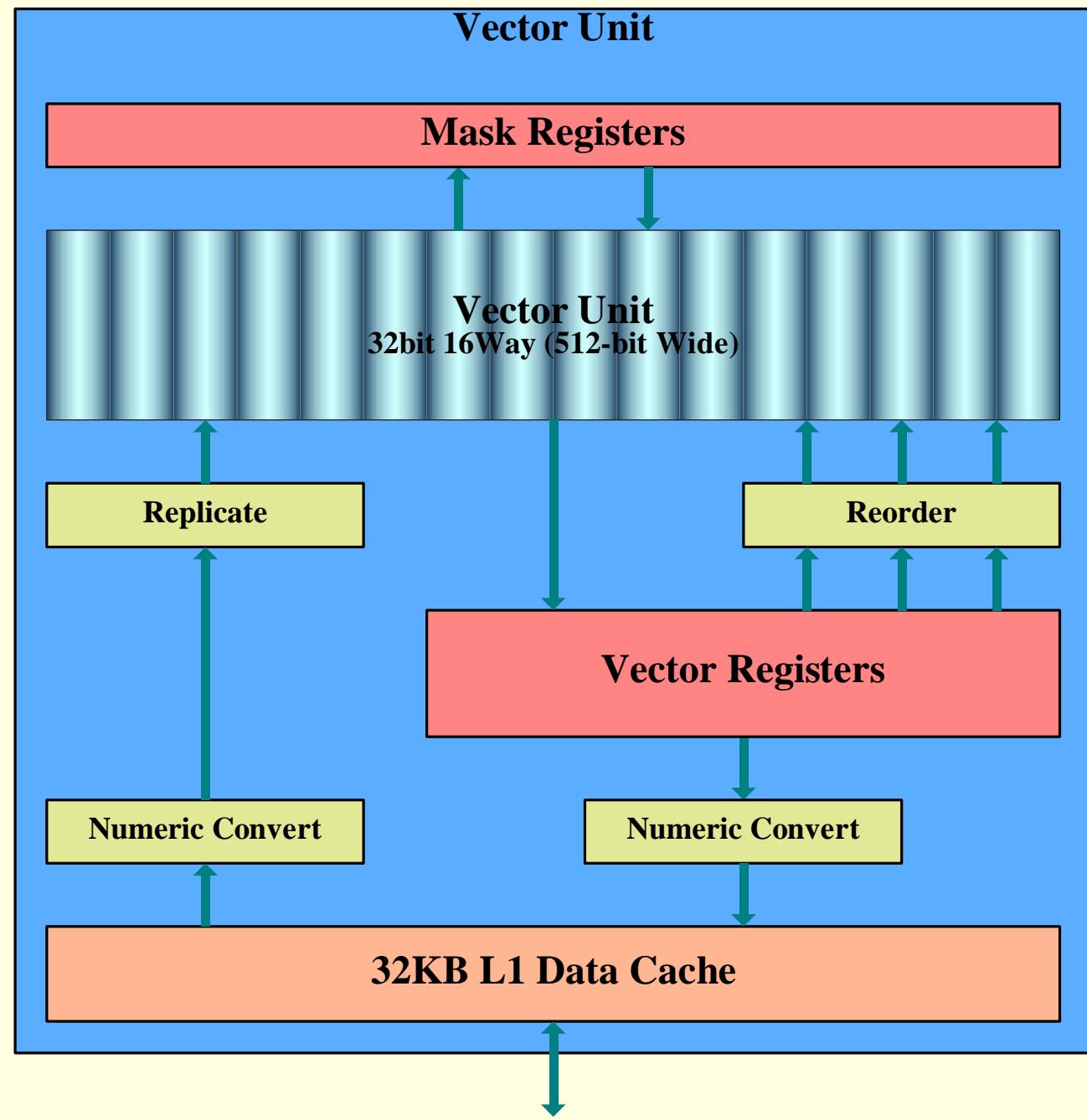


Larrabee Vector Unit Block Diagram



Vector complete instruction set
Scatter/gather for vector load/store
Mask registers select lanes to write
(for data-parallel flow control)
A separate execution kernel to each VPU lane

Vector instructions support
Fast read from L1 cache
Numeric type conversion and data replication
(read path from memory)
Rearrange the lanes on register read
Fused multiply add (three arguments)
Int32, Float32 and Float64 data