Tiled Design & Mesh Network

Repeated Tile Method:

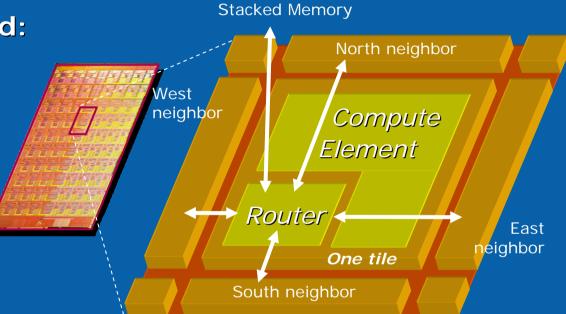
- Compute + router
- Modular, scalable
- Small design teams
- Short design cycle

Mesh Interconnect:

- "Network-on-a-Chip"
 - Cores networked in a grid allows for super high bandwidth communications in and between cores
- 5-port, 80GB/s* routers
- Low latency (1.25ns*)

Sunday, February 11th Noon PST

Future: connect IA/or and special purpose cores



To Future



^{*} When operating at a nominal speed of 4GHz Content under media embargo through